IN THE CLAIMS

1.-6. (canceled)

7. (new): A method for manufacturing a semiconductor device comprising;

preparing a plurality of semiconductor chips each including an electrode pad electrically connected to an integrated circuit and a conducting part electrically connected to the electrode pad, wherein the electrode pad and the conducting part are formed on a front side of each of the semiconductor chips;

arranging the semiconductor chips so as to dispose a clearance between the plurality of the semiconductor chips at predetermined intervals;

filling an insulating material on the front side of each of the semiconductor chips and in the clearance between the semiconductor chips so as to expose a part of the conducting part;

forming a through hole in the insulating material at a position of the clearance;

forming a conductive pattern to extend from an inner wall of the through hole to the conducting part of the semiconductor chip; and

cutting the insulating material along the through hole and separating the plurality of the semiconductor chips into individual pieces.

8. (new): The method according to claim 7, wherein the insulating material is resin.

9. (new): The method according to claim 7, wherein the through hole is formed by laser irradiation.

10. (new): The method according to claim 7, further including forming a solder resist on the front side of each of the semiconductor chips so as to cover apart of the conductive pattern.

11. (new): The method according to claim 7, further including forming a solder ball on the conductive pattern of each of the semiconductor chips.

12. (new): The method according to claim 7, including detaching the semiconductor chips prior to the step of arranging the semiconductor chips, and wherein the step of arranging the semiconductor chips comprises disposing the plurality of the semiconductor chips to create the clearance at the predetermined intervals.

13. (new): The method according to claim 7, wherein the step of filling an insulating material on the front side of each of the semiconductor chips and in the clearance between the semiconductor chips so as to expose a part of the conducting part comprises a single step.

14. (new): The method according to claim 7, wherein the steps are performed in the sequence in which they are recited.

15. (new): The method according to claim 7, wherein no insulating material is filled into the through hole.

16. (new): The method according to claim 7, comprising utilizing the conductive pattern as a connecting terminal.